Claim Amendments

1. (currently amended) An apparatus comprising:

a programmable logic device, arranged and constructed to receive a program that programs at least one processor operation and a variable clock speed into the programmable logic device;

at least one interface device through which the program and the variable clock speed are programmed into the programmable logic device;

wherein the programmable logic device is arranged and constructed to adjust the variable clock speed during execution of the at least one processor operation.

2. (original) The apparatus of claim 1, wherein the programmable logic device has as many pins as a processor for which the at least one processor operation is emulated.

3. (currently amended) The apparatus of claim 1, wherein the programmable logic device is further arranged and constructed to emulate the at least one processor operation repeatedly without interruption from one or more cyclical processor operations other than the at least one operation of the processor.

4. (currently amended) A method comprising the steps of:

selecting an operation that emulates at least one operation of a processor;

downloading the operation into a programmable logic device;

selecting a clock speed at which to operate the programmable logic device;

programming the programmable logic device to operate at the clock speed;

repeatedly testing the operation in combination with a circuit;

adjusting the clock speed during the step of repeatedly testing the operation in combination with the circuit.

5. (currently amended) The method of claim 4, wherein the step of testing is performed in isolation of cyclical operations other than the at least one operation of ~~a~~ the processor.

6. (original) The method of claim 4, wherein the operation is one of read/write byte, read/write word, read/write double word, read/write quad word, burst read, burst write, dynamic memory access, protocol stack, interrupt process, and protected mode.

7. (canceled)

8. (original) The method of claim 4, further comprising the step of pre-loading at least one operation into the programmable logic device.

9. (original) The method of claim 4, further comprising the steps of determining whether the operation is loaded into the programmable logic device and when the operation is loaded into the programmable logic device, omitting the downloading step.

10. (currently amended) The method of claim 4, further comprising the step of forwarding test data to the programmable logic device.

11. (currently amended) The method of claim 4, further comprising the step of returning test results to a user.

12. (original) The method of claim 4, wherein the method steps are implemented as computer readable program code within a computer-readable signal-bearing medium.

13. (currently amended) A computer-readable signal-bearing medium comprising:

computer readable program code for downloading one or more processor operations into a programmable logic device;

computer readable program code for selecting one of the one or more processor operations;

computer readable program code for selecting a clock speed at which to operate the programmable logic device;

computer readable program code for programming the programmable logic device to operate at the clock speed; ~~and~~

computer readable program code for repeatedly executing the selected one of the one or more processor operations; and

computer readable program code for adjusting the clock speed while repeatedly executing the selected one of the one or more processor operations.

14. (original) The computer-readable signal-bearing medium of claim 13, further comprising:

computer readable program code for determining whether the selected one of the one or more processor operations is downloaded into the programmable logic device; and

computer readable program code for downloading the selected one of the one or more processor operations into the programmable logic device when the selected one of the one or more processor operations is not downloaded into the programmable logic device.

15. (currently amended) The computer-readable signal-bearing medium of claim 13, wherein the computer readable program code for repeatedly executing the selected one of the one or more processor operations executes in isolation of cyclical operations other than the selected one of the one or more processor operations.

16. (original) The computer-readable signal-bearing medium of claim 13, wherein the selected one of the one or more processor operations is one of read/write byte, read/write word, read/write double word, read/write quad word, burst read, burst write, dynamic memory access, protocol stack, interrupt process, and protected mode.

17. (canceled)

18. (original) The computer-readable signal-bearing medium of claim 13, further comprising computer readable program code for pre-loading at least one operation into the programmable logic device.

19. (original) The computer-readable signal-bearing medium of claim 13, further comprising computer readable program code for forwarding test data to the programmable logic device.

20. (original) The computer-readable signal-bearing medium of claim 13, further comprising computer readable program code for returning test results to a user.

21. (new) The method of claim 4, wherein the step of repeatedly testing the operation in combination with the circuit comprises the step of:

repeatedly testing the operation without waiting through processor operation cycles that do not provide the operation.

22. (new) The computer-readable signal-bearing medium of claim 13, wherein the computer readable program code for repeatedly executing the selected one of the one or more processor operations comprises:

computer readable program code for repeatedly executing the selected one of the one or more processor operations without waiting through one or more other processor operations of a processor operation cycle that do not provide the selected one of the one or more processor operations.